19-2623; Rev 0; 1/03

EVALUATION KIT AVAILABLE

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

General Description

The MAX1955/MAX1956 are dual-output, fixed-frequency, voltage-mode, pulse-width modulated (PWM) step-down controllers with 0.5% output accuracy. Each controller switches at a constant 600kHz and is 180° out-of-phase with the other controller, reducing input ripple current and the number of input capacitors.

An on-chip bias supply generates a 5V gate drive to deliver up to 25A output current per phase with low-cost N-channel MOSFETs at up to 93% efficiency. Lossless adjustable current limit eliminates expensive current-sense resistors and improves efficiency. Foldback current limit reduces power dissipation during short-circuit conditions and handles transient overloads better than controllers using hiccup-mode short-circuit protection.

Output voltage margining shifts output voltage by ±4% from the nominal value to simplify system test. Outputs also can be powered up and down in selectable sequences to meet core and logic supply-rail requirements.

The MAX1955/MAX1956 are available in a 28-lead thin QFN package with exposed pad.

Applications

Base Stations

Telecom and Network Equipment

Servers

DSP, ASIC, µP, and FPGA Supplies

Features

- **Operates from a 1.6V to 5.5V Supply (MAX1956)**
- **0.5% Output Accuracy**
- **0.8V to 0.9V_{IN} Output Range**
- **Up to 25A per Phase Output Current**
- **On-Chip Boost Regulator Provides 5V Gate Drive**
- **Up to 93% Efficiency**
- **180° Out-of-Phase Operation**
- **±4% Voltage Margining**
- **Lossless, Foldback Current Limit**
- **Selectable Voltage Sequencing**
- **Synchronizable to External Clock**
- **Digital Soft-Start and Soft-Stop**
- **Small 28-Pin, 5mm × 5mm Thin QFN Package**

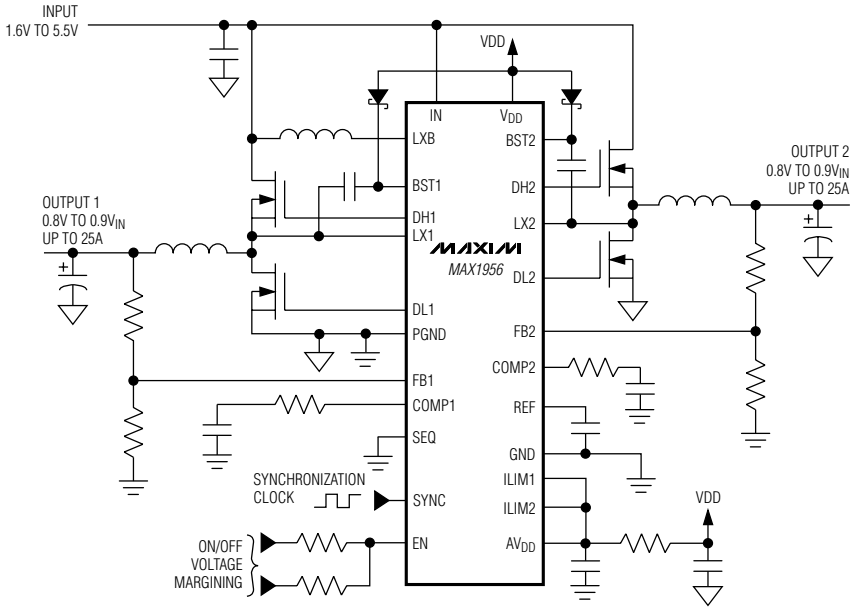
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1955ETI	-40°C to +85°C	28 Thin QFN-EP*
MAX1956ETI	-40°C to +85°C	28 Thin QFN-EP*

**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

ABSOLUTE MAXIMUM RATINGS

IN, AVDD, SYNC, EN, ILIM_, FB_, SEQ to GND .....-0.3V to +6V
COMP_, REF to GND .....-0.3V to (V_{AVDD} + 0.3V)
LXB to GND .....-0.3V to (V_{VDD} + 0.3V)
DL_ to GND .....(V_{PGND} - 0.3V) to (V_{VDD} + 0.3V)
BST_ to GND .....-0.3V to +12V
DH1 to LX1 .....-0.3V to (BST1 + 0.3V)
DH2 to LX2 .....-0.3V to (BST2 + 0.3V)
LX1 to BST1 .....-6V to +0.3V
LX2 to BST2 .....-6V to +0.3V
PGND to GND or VDD to AVDD .....-0.3V to +0.3V
REF Short-Circuit to GND .....Continuous
I_{VDD} 250mA
Continuous Power Dissipation* (T_A = +70°C)
28-Lead Thin QFN
(derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

**Exposed pad soldered to PC board.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = 3.3V; V_{VDD} = V_{AVDD} = 5V; V_{PGND} = V_{GND} = 0; C_{REF} = 0.22µF; SEQ = SYNC = GND; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Input Voltage Range	MAX1955		2.25		5.50	V
	MAX1956 (Note 1)		1.6		5.5	
IN Input Voltage UVLO	Rise or fall	MAX1955, hysteresis = 35mV	1.9		2.2	V
		MAX1956, hysteresis = 30mV	1.30		1.58	
FB Regulation Voltage			0.796	0.8	0.804	V
FB Regulation Voltage with Positive Voltage Margining	Percentage change from nominal regulation voltage		3	4	5	%
FB Regulation Voltage with Negative Voltage Margining	Percentage change from nominal regulation voltage		-5	-4	-3	%
Line Regulation Error	Note 2			0.1	0.3	%
Feedback Input Bias			-0.2		+0.2	µA
Feedback Transconductance			1	2	3	mS
COMP Source Current			100	150		µA
COMP Sink Current			100	150		µA
COMP Pulldown Resistance	In shutdown				100	Ω
Output Soft-Start Time				4.27		ms
Step-Down Switching Frequency	SYNC = GND (Note 3)		540	600	660	kHz
SYNC Frequency Range	2 times step-down switching frequency		1080		1320	kHz
Maximum Duty Cycle	Measured at DH_		90	93	97	%
Minimum Duty Cycle	Measured at DH_			7	10	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = 3.3V; V_{VDD} = V_{AVDD} = 5V; V_{PGND} = V_{GND} = 0; C_{REF} = 0.22µF; SEQ = SYNC = GND; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} No-Load Supply Current	Total of VDD1 + VDD2 + AVDD current, SYNC = GND, no load on DH_ or DL_			20	32	mA
IN Supply Current				35	100	µA
IN Shutdown Supply Current					20	µA
REF Voltage			1.267	1.28	1.293	V
REF Load Regulation	I_{REF} = -50µA to +50µA				0.01	V
Default Current-Limit Threshold	ILIM_ = V_{DD}, measured from PGND to LX_		127.5	150	172.5	mV
Adjustable Current-Limit Threshold	Measured from PGND to LX_	$R_{ILIM\_}$ = 100kΩ	60	75	90	mV
		$R_{ILIM\_}$ = 400kΩ	240	300	360	
Thermal-Shutdown Threshold	T_J rising, 15°C hysteresis			160		°C
DH_ Gate-Driver On-Resistance	Pulling up or down			1	1.8	Ω
DL_ Gate-Driver Pullup On-Resistance	DL_ high state			1	1.8	Ω
DL_ Gate-Driver Pulldown On-Resistance	DL_ low state			0.35	0.65	Ω
Dead Time (Adaptive)	DH_ falling to DL_ rising			23		ns
	DL_ falling to DH_ rising			26		
SYNC Minimum Pulse Width	High or low		200			ns
EN Voltage Range for Nominal Output Voltage	Percentage of V_{IN}		80	90	100	%
EN Voltage Range for Positive Voltage Margining	Percentage of V_{IN}		55		70	%
EN Voltage Range for Negative Voltage Margining	Percentage of V_{IN}		30		45	%
EN Voltage Range for Shutdown	Percentage of V_{IN}		0		20	%
EN, SEQ, SYNC Input High Voltage	(Note 4)		V_{IN} - 0.5			V
SEQ, SYNC Input Low Voltage					0.5	V
EN, SEQ, SYNC Input Current			-1		+1	µA
BST_ Leakage Current in Shutdown			-20		+20	µA
V_{DD} Output Voltage	I_{VDD} = 0 to 150mA		4.75		5.50	V

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = 3.3V; V_{VDD} = V_{AVDD} = 5V; PGND = GND = 0; C_{REF} = 0.22µF; SYNC = GND; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Input Voltage Range	MAX1955		2.25		5.50	V
	MAX1956 (Note 1)		1.6		5.5	
IN Input Voltage UVLO	Rise or fall	MAX1955	1.9		2.2	V
		MAX1956	1.30		1.58	
FB Regulation Voltage			0.794		0.806	V
FB Regulation Voltage with Positive Voltage Margining	Percentage change from nominal regulation voltage		+3		+5	%
FB Regulation Voltage with Negative Voltage Margining	Percentage change from nominal regulation voltage		-5		-3	%
Line Regulation Error	(Note 2)				0.3	%
FB_ Input Bias			-0.2		+0.2	µA
Feedback Transconductance			1.0		3.1	mS
COMP_ Source Current			100			µA
COMP_ Sink Current			100			µA
COMP_ Pulldown Resistance	In shutdown				100	Ω
Step-Down Switching Frequency	SYNC = GND (Note 3)		540		660	kHz
SYNC Frequency Range	2 times step-down switching frequency		1080		1320	kHz
Maximum Duty Cycle	Measured at DH_		90		97	%
Minimum Duty Cycle	Measured at DH_				10	%
V_{DD} Quiescent Supply Current	Total of VDD1 + VDD2 + AVDD current, SYNC = GND, no load on DH_ or DL_				32	mA
IN Quiescent Supply Current					100	µA
IN Shutdown Supply Current					20	µA
REF Voltage			1.267		1.293	V
REF Load Regulation	I_{REF} = -50µA to +50µA				0.01	V
Default Current-Limit Threshold	ILIM_ = V_{DD}; measured from PGND to LX_		127.5		172.5	mV
Adjustable Current-Limit Threshold	Measured from PGND to LX_	$R_{ILIM\_}$ = 100kΩ	60		90	mV
		$R_{ILIM\_}$ = 400kΩ	240		360	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = 3.3V; V_{VDD} = V_{AVDD} = 5V; PGND = GND = 0; C_{REF} = 0.22µF; SYNC = GND; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DH_ Gate-Driver On-Resistance	Pulling up or down			1.8	Ω
DL_ Gate-Driver Pullup On-Resistance	DL_ high state			1.8	Ω
DL_ Gate-Driver Pulldown On-Resistance	DL_ low state			0.65	Ω
SYNC Minimum Pulse Width	High or low	200			ns
EN Voltage Range for Nominal Output Voltage	Percentage of V_{IN}	80		100	%
EN Voltage Range for Positive Voltage Margining	Percentage of V_{IN}	55		70	%
EN Voltage Range for Negative Voltage Margining	Percentage of V_{IN}	30		45	%
EN Voltage Range for Shutdown	Percentage of V_{IN}	0		20	%
EN, SEQ, SYNC Input High Voltage	(Note 4)	V_{IN} - 0.5			V
SEQ, SYNC Input Low Voltage				0.5	V
EN, SEQ, SYNC Input Current		-1		+1	µA
BST_ Leakage Current in Shutdown		-20		+20	µA
V_{DD} Output Voltage	I_{VDD} = 0 to 150mA	4.75		5.50	V

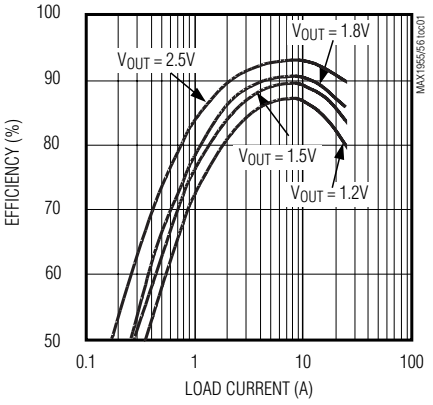
Note 1: IN input voltage must not drop below minimum voltage because of ripple or transient conditions.
Note 2: Guaranteed by design.
Note 3: Boost frequency is 2x step-down frequency.
Note 4: For proper startup, EN must exceed V_{IN} - 0.5V.
Note 5: Specifications to -40°C are guaranteed by design but not production tested.

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

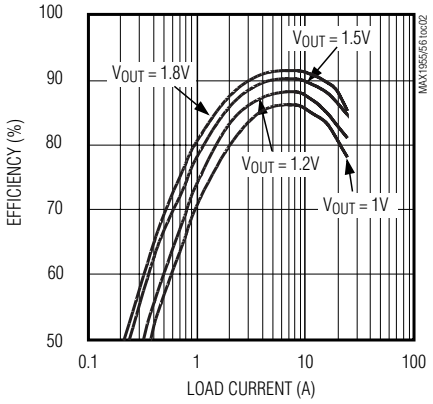
Typical Operating Characteristics

(Circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

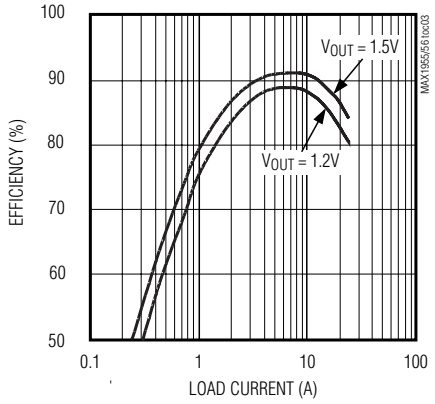
EFFICIENCY vs. LOAD CURRENT WITH 3.3V INPUT



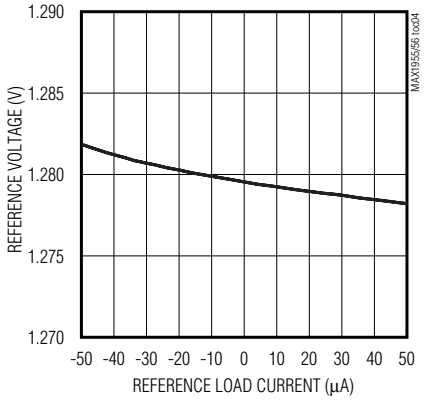
EFFICIENCY vs. LOAD CURRENT WITH 2.5V INPUT



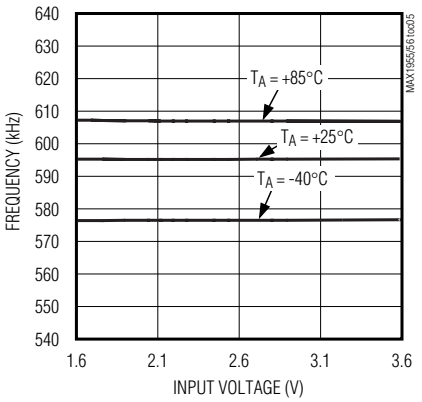
MAX1956 EFFICIENCY vs. LOAD CURRENT WITH 1.8V INPUT



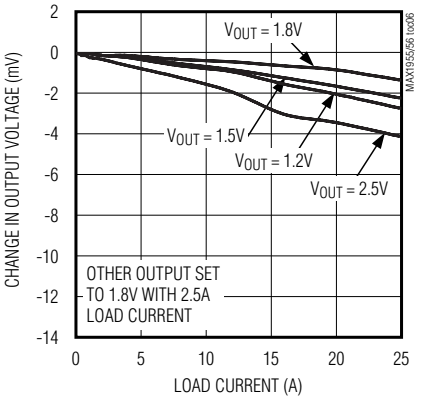
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



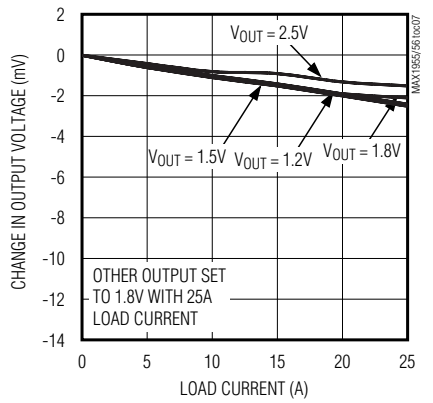
STEP-DOWN SWITCHING FREQUENCY vs. INPUT VOLTAGE



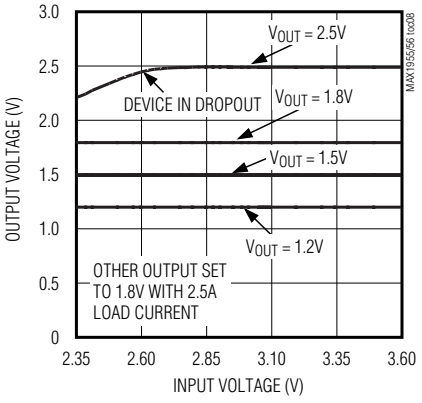
CHANGE IN OUTPUT VOLTAGE vs. LOAD CURRENT WITH 3.3V INPUT



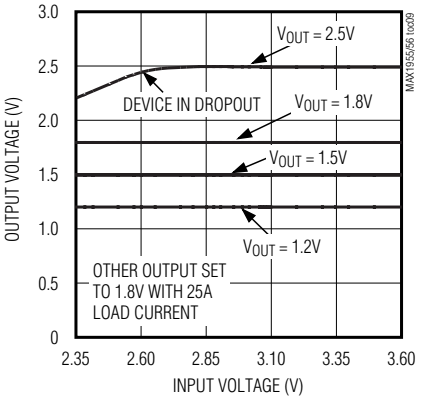
CHANGE IN OUTPUT VOLTAGE vs. LOAD CURRENT WITH 3.3V INPUT



OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH NO LOAD



OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH NO LOAD

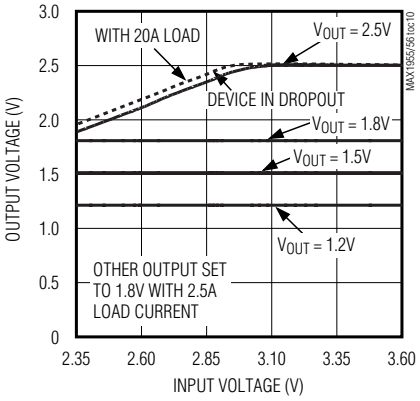


1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

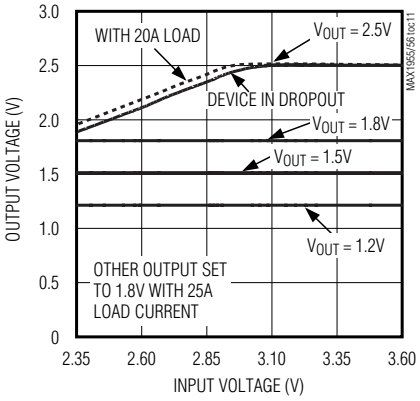
Typical Operating Characteristics (continued)

(Circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

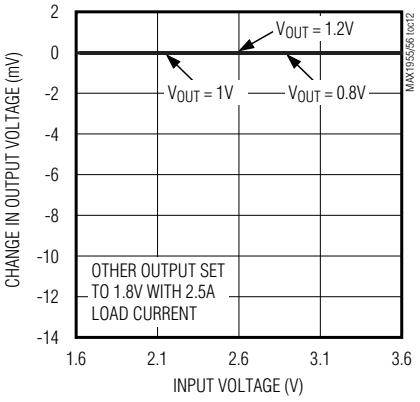
OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH 25A LOAD



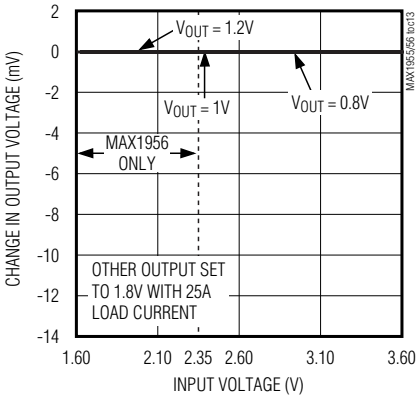
OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH 25A LOAD



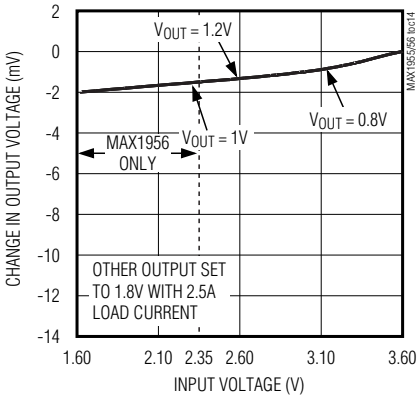
MAX1956 CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH NO LOAD



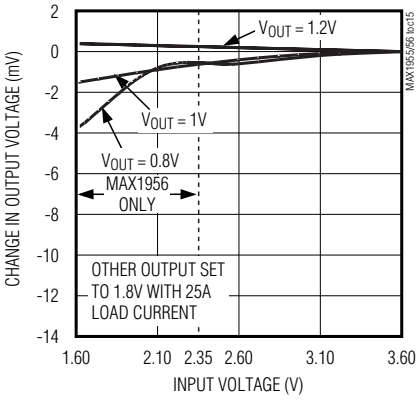
CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH NO LOAD



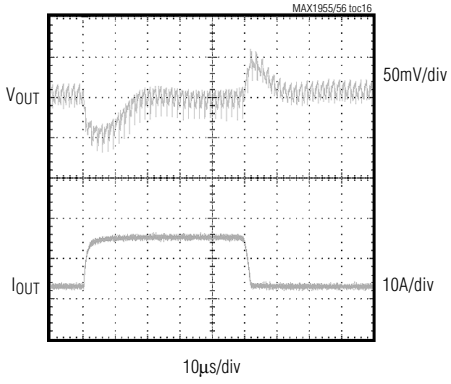
CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH 25A LOAD



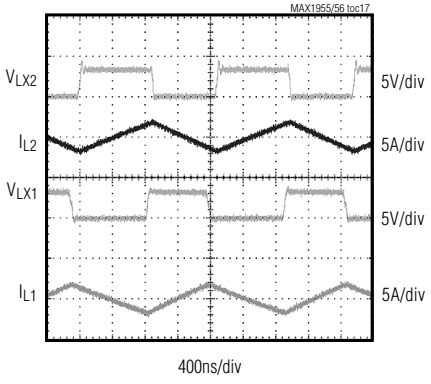
CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH 25A LOAD



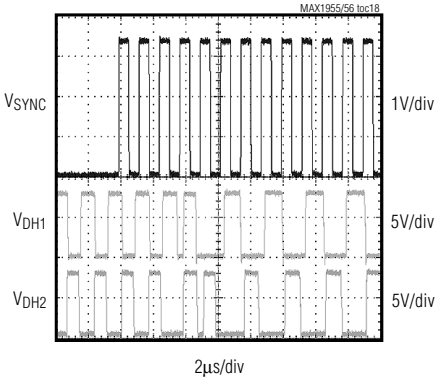
LOAD TRANSIENT WITH 1.5V OUTPUT



SWITCHING WAVEFORMS



SYNCHRONIZATION WAVEFORMS

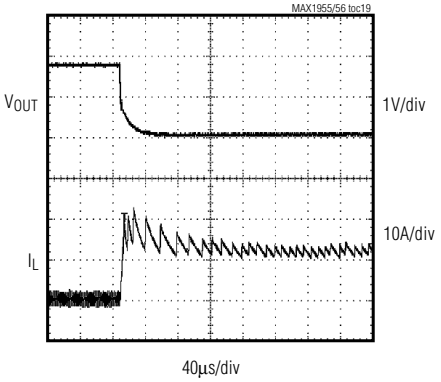


1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

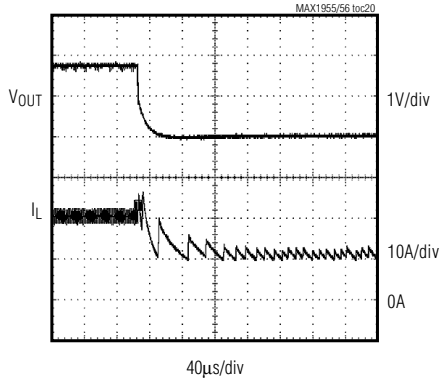
Typical Operating Characteristics (continued)

(Circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

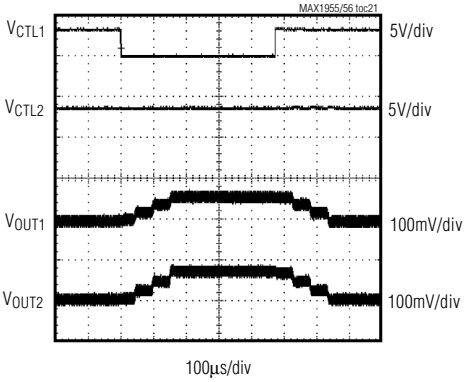
NO LOAD TO SHORT CIRCUIT



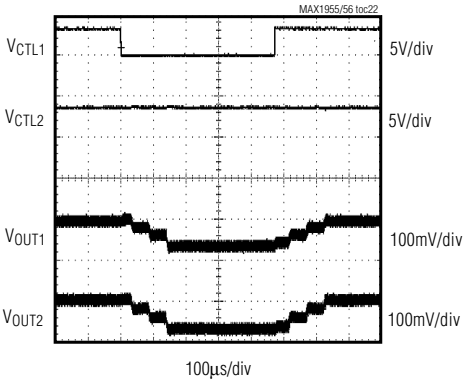
20A LOAD TO SHORT CIRCUIT



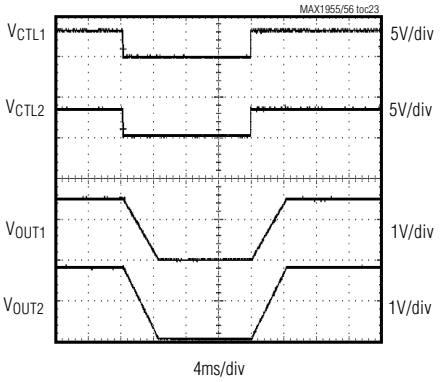
HIGH OUTPUT MARGINING



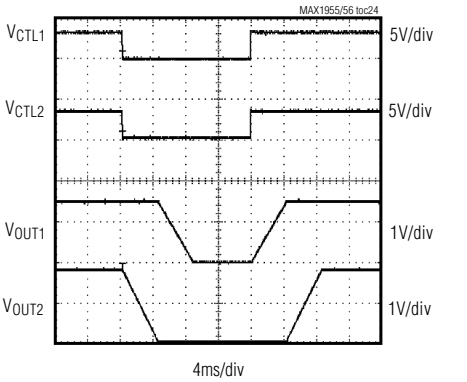
LOW-OUTPUT MARGINING



SHUTDOWN/STARTUP WITH SEQ = GND



SHUTDOWN/STARTUP WITH SEQ = AV_{DD}



Pin Description

PIN	NAME	FUNCTION
1	DL1	Low-Side MOSFET Gate-Driver Output. Connect to the low-side MOSFET gate. DL1 is pulled low in shutdown.
2	LX1	Inductor Connection. Connect to the switched side of the inductor.
3	DH1	High-Side MOSFET Gate-Driver Output. Connect to the high-side MOSFET gate. DH1 is pulled low in shutdown.
4	BST1	High-Side MOSFET Gate-Driver Bootstrap Connection. Connect a capacitor from BST1 to LX1 and a Schottky diode from V_{DD} to BST1.
5	SYNC	Frequency Synchronization Input. Connect to GND for normal 600kHz operation, or drive with a clock signal from 1080kHz to 1320kHz. The two step-down regulators are synchronized to alternating clock pulses, resulting in 180° out-of-phase operation at half the synchronization frequency.

Pin Description (continued)

PIN	NAME	FUNCTION
6	EN	Enable and Voltage Margining Input. Connect EN to IN for normal operation or connect to GND for shutdown. Set V_{EN} = (1/3)V_{IN} to set the outputs to -4% of nominal. Set V_{EN} = (2/3)V_{IN} to set the outputs to +4% of nominal (see the *Shutdown and Output Voltage Margining (EN)* section).
7	ILIM1	Current-Limit Adjust. Sets the threshold for current sensing across the low-side MOSFET's $R_{DS(ON)}$. Connect ILIM1 to AV_{DD} for a 150mV threshold. For adjustable constant current or foldback current-limit setting, see the *Current Limit* section.
8	FB1	Feedback Input. Connect to a voltage-divider from the output to GND to set the output voltage (see the *Setting the Output Voltage* section).
9	COMP1	Compensation. Internally pulled to ground during shutdown (see the *Compensation Design* section).
10	GND1	Ground. Connect to the PC board analog ground plane. Connect PC board power ground plane and analog ground plane with a single connection.
11	REF	1.28V Reference. Connect a 0.22µF capacitor from REF to GND.
12	GND	Ground. Connect to the PC board analog ground plane. Connect the PC board power ground plane and analog ground plane with a single connection.
13	COMP2	Compensation. Internally pulled to ground during shutdown (see the *Compensation Design* section).
14	FB2	Feedback Input. Connect to a voltage-divider from the output to GND to set the output voltage (see the *Setting the Output Voltage* section).
15	ILIM2	Current-Limit Adjust. Sets the threshold for current sensing across the low-side MOSFET's $R_{DS(ON)}$. Connect ILIM2 to AVDD for a 150mV threshold. For adjustable constant current or foldback current-limit setting, see the *Current Limit* section.
16	AV_{DD}	Analog Supply Input. Connect a 10Ω resistor from V_{DD} to AV_{DD} and a 0.47µF capacitor from AV_{DD} to GND.
17	SEQ	Power-Sequence Input. Connect SEQ to GND to set OUT1 and OUT2 to power up and power down simultaneously. Connect SEQ to IN to make OUT1 power up first and power down last.
18	BST2	High-Side MOSFET Gate-Driver Bootstrap Connection. Connect a capacitor from BST2 to LX2 and a Schottky diode from V_{DD} to BST2.
19	DH2	High-Side MOSFET Gate-Driver Output. Connect to the high-side MOSFET gate. DH2 is pulled low in shutdown.
20	LX2	Inductor Connection. Connect to the switched side of the inductor.
21	DL2	Low-Side MOSFET Gate-Driver Output. Connect to the low-side MOSFET gate. DL2 is pulled low in shutdown.
22	PGND2	Power Ground. Connect to the low-side MOSFET source for regulator 2 and PC board power ground plane.
23	IN	Input Supply
24	V_{DD2}	Internal Boost Regulator Output. Connect to V_{DD1}, and bypass with a 10µF capacitor to GND.
25	LXB	Internal Boost Regulator Inductor Connection. Connect a 4.7µH inductor from LXB to IN. Internally shorted to V_{DD2} in shutdown.
26	PGND	Power Ground. Connect to PC board power ground plane.
27	V_{DD1}	Internal Boost Regulator Output. Connect to V_{DD2}.
28	PGND1	Power Ground. Connect to the low-side MOSFET source for regulator 1 and PC board power ground plane.
Exposed Pad	—	Exposed Pad. Solder to the PC board analog ground plane for optimum power dissipation.

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

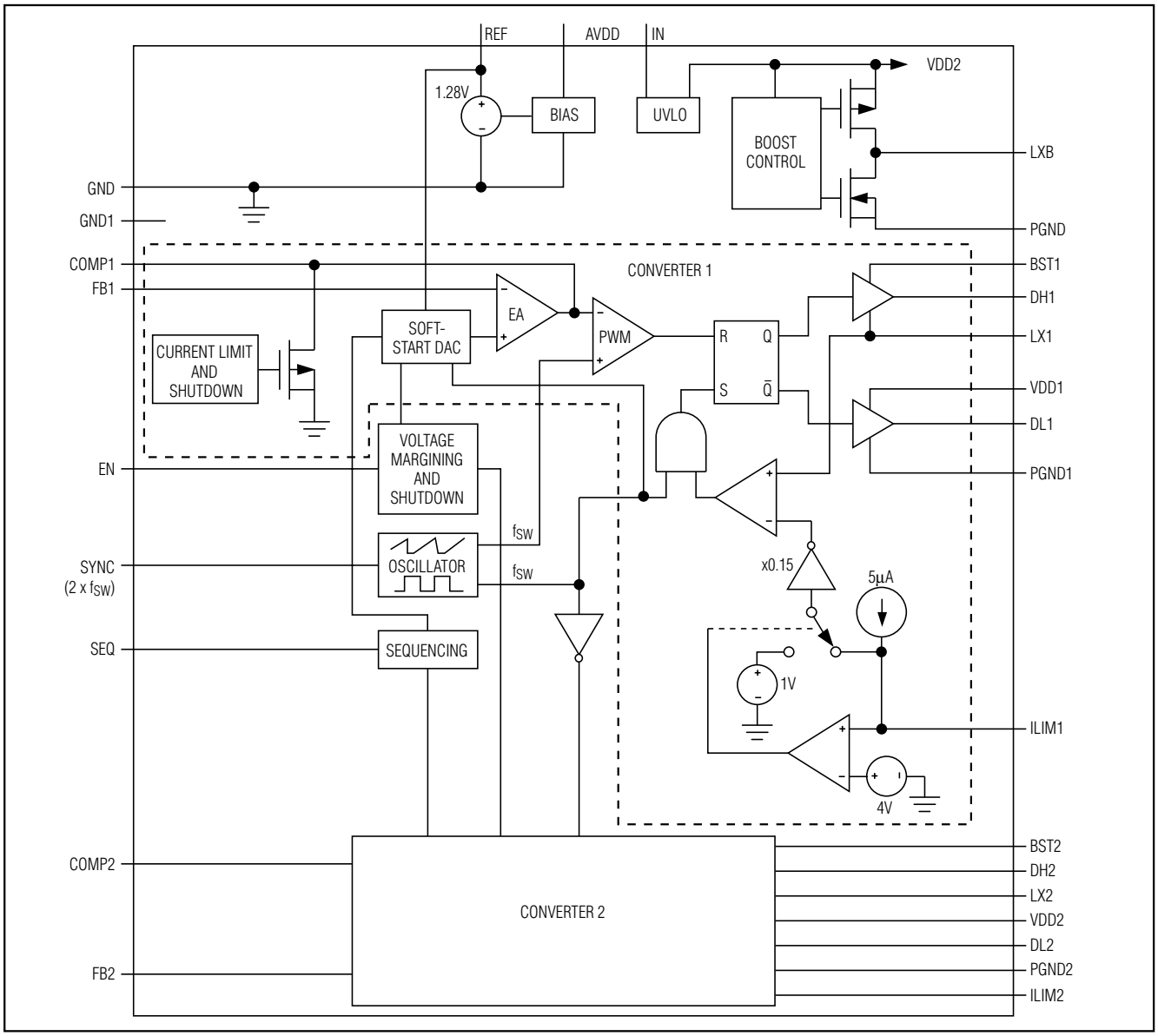


Figure 1. Functional Diagram

Detailed Description

The MAX1955/MAX1956 are dual-output, fixed-frequency, voltage-mode, PWM step-down controllers with 0.5% output accuracy. Each controller switches at a constant 600kHz and is 180° out-of-phase with the other controller, which reduces input ripple current and the number of input capacitors. Figure 1 is the functional diagram.

An on-chip step-up bias supply generates a 5V gate drive to deliver up to 25A output current per phase with low-cost N-channel MOSFETs at up to 93% efficiency. Lossless adjustable current limit eliminates expensive current-sense resistors and improves efficiency. Foldback current limit reduces power dissipation during short-circuit condition and handles transient overloads better than controllers using hiccup-mode short-circuit protection.

Output voltage margining shifts the output voltage by ±4% from the nominal value to simplify system testing. Outputs also can be powered up and down in selectable sequences to meet core and logic supply rail requirements.

DC-to-DC PWM Controller

The MAX1955/MAX1956 step-down DC-to-DC converters use a PWM voltage-mode control scheme. The controller generates the clock signal by dividing down the internal oscillator (or SYNC signal when using an external clock) so that each controller's switching frequency equals 1/2 the oscillator frequency. An internal transconductance error amplifier produces an integrated error voltage at the COMP_ pin, providing high DC accuracy. The voltage at COMP sets the duty cycle, using a PWM comparator and a ramp generator. At the rising edge of the clock, Regulator 1's high-side N-channel MOSFET turns on and remains on until either the appropriate duty cycle or the maximum duty cycle is reached. Regulator 2 operates out of phase, so its high-side MOSFET turns on at the falling edge of the clock. During the on-time of each high-side MOSFET, the associated inductor current ramps up.

During the second half of the switching cycle, the high-side MOSFET turns off and the low-side N-channel MOSFET (synchronous rectifier) turns on. The inductor releases its stored energy as its current ramps down, providing current to the load.

High-Side Gate-Drive Supply (BST)

The gate-drive voltage for the high-side N-channel switch is generated by a flying capacitor. This capacitor between BST and LX is alternately charged from the V_{DD} supply and placed in parallel to the high-side MOSFET's gate and source terminal through the high-side driver.

On startup, the low-side MOSFET forces LX to ground and charges the boost capacitors to V_{DD} through the Schottky diodes (D1 and D2 of Figure 5). On the second half cycle, the controller turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary gate-to-source voltage to turn on the high-side MOSFET, an action that boosts the 5V gate-drive signal above the input voltage.

Current Limit

The current-limit circuit employs a "valley" current-sensing algorithm that uses the on-resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal (measured from PGND_ to LX_) is above the current-limit threshold, the MAX1955/MAX1956 do not initiate a new cycle, and COMP_ is pulled to ground. Since valley current sensing is used, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current (Figure 2). The exact current-limit characteristic and maximum load capacity are a function of the low-side MOSFET's on-resistance, the current-limit threshold, the inductor value, and the input voltage. This provides a robust lossless current sense that does not require current-sense resistors.

An added feature is the implementation of Schottky diodes D3 and D4 (as shown in Figure 5), which reduce output short-circuit currents.

Constant-Current Limit

The adjustable current limit accommodates MOSFETs with a wide range of on-resistance values. The current-limit threshold is adjusted with an external resistor connected from ILIM_ to GND ($R_{ILIM\_}$). The adjustment range is 75mV to 300mV, measured across the low-side MOSFET. The value of $R_{ILIM\_}$ is calculated using the following formula:

$$R_{ILIM\_} = \frac{I_{VALLEY}}{0.15 \times 5\mu A} \times R_{DS(ON)}$$

where I_{VALLEY} is the valley current limit and $R_{DS(ON)}$ is the on-resistance of the low-side MOSFET. To avoid reaching the current limit at a lower current than expected, use the maximum value for $R_{DS(ON)}$ at an elevated junction temperature. Refer to the MOSFET manufacturer's data sheet for maximum values.

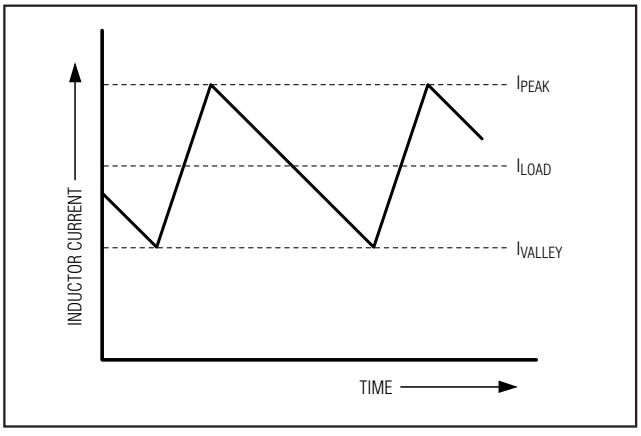


Figure 2. Inductor Current Waveform

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

Foldback Current Limit

Foldback current limit is used to reduce power dissipation during overload and short-circuit conditions. This is accomplished by lowering the current-limit threshold as the output voltage drops because of overload.

To use foldback current limit, connect one resistor (R_{FOBK}) from ILIM_ to the corresponding output, and connect another resistor (R_{ILIM}) from ILIM_ to GND. The values of R_{ILIM} and R_{FOBK} are calculated as follows:

1) First, select the percentage of foldback (P_{FB}). This percentage corresponds to the current limit when V_{OUT} equals zero, divided by the current limit when V_{OUT} equals its nominal voltage. Typical values are 15% to 30%. To solve for the resistor values, use the following equations:

$$R_{FOBK} = \frac{P_{FB} \times V_{OUT}}{5\mu A(1 - P_{FB})}$$

$$R_{ILIM} = \frac{6.67 \times R_{DS(ON)} \times I_{VALLEY} \times (1 - P_{FB}) \times R_{FOBK}}{V_{OUT} - \left(6.67 \times R_{DS(ON)} \times I_{VALLEY} \times (1 - P_{FB})\right)}$$

2) Select P_{FB} values that provide R_{ILIM} greater than zero.

Recovery from Overload and Short Circuit

The MAX1955/MAX1956 do not recover to nominal output voltage at heavy load (near full load) after an overload or short-circuit condition, but they might operate at a voltage below the nominal output until the input power or EN pin is cycled through the OFF state. If automatic recovery is mandatory, without cycling EN or input power, add an RC filter of 1Ω and 0.015µF at LX_'s pins, as shown in Figure 6. Doing so decreases the efficiency by 2% to 3%, depending on the input voltage, output voltage, and current.

AVDD Decoupling

Due to high switching frequency and tight output tolerance (±0.5%), decoupling between V_{DD} and AV_{DD} is recommended. Connect a 10Ω resistor between V_{DD} and AV_{DD} and a 0.47µF capacitor between AV_{DD} and GND. Place the capacitor as close to AV_{DD} as possible.

Undervoltage Lockout (UVLO)

When the voltage at IN drops below its undervoltage lockout (UVLO) threshold (see the *Electrical Characteristics*), the MAX1955/MAX1956 determine that the input supply voltage is too low to power the IC. In this event, the main outputs and the internal boost regulator are disabled. The boost regulator starts up again once the voltage at IN rises above the UVLO threshold.

Startup and Output Sequencing

The MAX1955/MAX1956 use a digital soft-start to reduce input inrush current during startup. In soft-start, the output voltage is ramped up by increasing the FB_ regulation voltage in 80 steps of 10mV. Total soft-start time is typically 4.27ms.

Some power supplies exhibit soft regulation during soft-start. If the MAX1955/MAX1956 are powered from such a power supply and enabled at or before power-up, the input voltage might dip below the UVLO threshold, and the output might not soft-start properly. To avoid such issues, enable the MAX1955/MAX1956 after the input supply has stabilized or add an RC filter to the IN pin of the IC as shown in Figure 6. The value of R20 is ~510Ω, and the value of capacitor C31 is from 1µF to 10µF, depending on the startup characteristic of the input power supply. The capacitor value is chosen to provide power to the IC (100µA max) and keep it from falling below the UVLO threshold during the input power-supply dip.

The outputs can be set to power up at the same time, or output 1 can be set to power up first and power down last. Connect SEQ to GND for simultaneous power up/down. Connect SEQ to IN to make output 1 power up first and power down last. Figure 3 is a timing diagram.

If there is a fault condition (such as a short circuit) on output 1 causing its voltage to drop below 90% of its nominal regulation voltage, and SEQ is connected to IN, then output 2 shuts down. Once the fault is cleared, allowing the voltage on output 1 to rise above 90% of its nominal regulation voltage, output 2 soft-starts and powers up again.

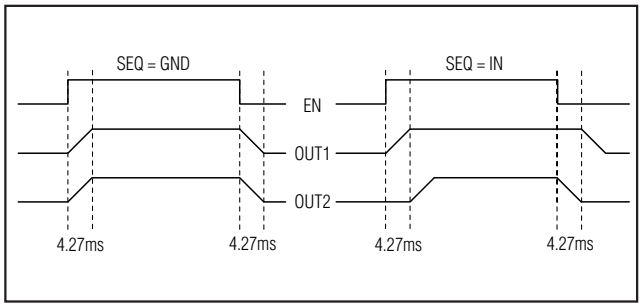


Figure 3. Timing Diagram

Synchronization

An external clock of 1080kHz to 1320kHz at SYNC forces the controller to switch at half of this clock frequency. DH1 and DH2 positive-going edges alternately synchronize to the rising edge of the external clock, thus operating 180° out-of-phase with each other. See the Synchronization and Switching Waveforms in the *Typical Operating Characteristics*.

Shutdown and Output Voltage Margining (EN)

The MAX1955/MAX1956 feature a low-power shutdown mode that reduces the IC's current consumption to less than 20µA. For normal operation, connect EN to IN. To place the part in low-current shutdown mode, connect EN to GND.

When the MAX1955/MAX1956 enter shutdown (EN goes low), soft-stop begins. In soft-stop, the output voltage is ramped down by lowering the FB_ regulation voltage to zero in 80 steps of 10mV. Total soft-stop time is typically 4.27ms.

Each controller can be shut down individually by pulling COMP_ to GND with an open collector NPN transistor (Figure 6). This shuts down the controller immediately without going through soft-stop. Once COMP_ is released, the controller powers up without going through soft-start. To protect against inrush current when using this power-up/-down method, use foldback current limit. Also, connect SEQ to GND to prevent output 2 from powering down when the voltage on output 1 drops.

In an effort to improve quality, many OEMs are testing their system's operation over the range of minimum and maximum supply voltage. To facilitate this testing, the MAX1955/MAX1956 have a voltage-margining feature that increases or decreases the output voltages by 4%.

The voltage on EN controls voltage margining. To increase the output voltage by 4%, apply (2/3) V_{IN} to EN. To reduce the output voltage by 4%, apply (1/3) V_{IN} to EN.

One easy way to use the voltage-margining feature is to make two control logic inputs (CTL1 and CTL2) by connecting two resistors to EN. Connect a 200kΩ resistor from EN to CTL1, and a 100kΩ resistor from EN to CTL2 (Figure 5). The voltage margining is then controlled by connecting CTL1 and CTL2 to IN or GND, as shown in Table 1. Before applying voltage-margining, pull VCTL1 and VCTL2 to > V_{IN} - 0.5V to ensure proper startup.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation of the MAX1955/MAX1956. When the junction temperature exceeds +160°C, an internal thermal sensor shuts down the device, allowing the IC to cool. The thermal sensor turns the device on after the junction temperature cools by 15°C. In a continuous thermal-overload condition, this results in a pulsed output.

Low-Side MOSFET Negative-Current Conduction

Under most operating conditions, the low-side MOSFET conducts only positive inductor currents that flow from source to drain and 1/2 of the inductor peak-to-peak ripple current (~15% full load current) in the negative direction when output is at no load. If the MAX1955/MAX1956 are disabled before their soft-start cycle is complete (~4ms), the converter is disabled without a soft-stop, and the output discharges through its load. In this case, if the converter is reenabled before the output capacitor discharges completely, the soft-start cycle resets the reference input to the error amp to zero and ramps up again.

The converter forces DL on until the feedback drops below the reference input. If the output is almost fully charged when the converter turns back on, a large negative current can build up in the inductor. If the negative current is excessive, a high LX voltage spike can occur because of parasitic circuit inductances as DL is released. This high LX voltage spike can shut down and latch off the circuit. To prevent this from happening, add a series resistor between DL and the gate of the low-side MOSFET (Figure 6) to slow down the turn-off di/dt, reducing the voltage spike and preventing the circuit from shutting down. A 1Ω resistor works fine for most applications without noticeable degrading impact on efficiency or Cdv/dt-induced turn-on effect.

Table 1. Voltage Margining

CTL1	CTL2	EN	OUTPUT
V_{IN}	V_{IN}	V_{IN}	Nominal
0	V_{IN}	(2/3)V_{IN}	+4%
V_{IN}	0	(1/3)V_{IN}	-4%
0	0	0	Shutdown

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

Design Procedure

Setting the Output Voltage

Output voltage is set with a resistor-divider, as shown in Figure 4. The output voltage can be set to as low as 0.8V. The maximum output voltage is limited by maximum duty cycle and external component selection. Select R_X (the resistor from FB to GND) between 8kΩ and 10kΩ, and calculate R_Y from:

$$R_Y = R_X \times \left(\frac{V_{OUT}}{0.8} - 1 \right)$$

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX1955/MAX1956: inductance value (L), peak inductor current (I_{PEAK}), and DC resistance (R_{DC}). A good compromise between size and efficiency is to set the inductor peak-to-peak ripple current equal to 30% of maximum load current, thus LIR = 0.3. The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{OUT(MAX)} \times LIR}$$

where f_{SW} is the switching frequency (typically 600kHz). The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, and also improve transient response, but reduce efficiency and increase output voltage ripple because of higher peak currents. Higher inductance increases efficiency by reducing the RMS current. However, resistive losses because of extra wire turns could exceed the benefit gained from lower AC current levels, especially when the inductance is increased without also allowing larger inductor dimensions.

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. The inductor's saturation current rating must exceed the peak inductor current at the maximum defined load current ($I_{LOAD(MAX)}$):

$$I_{PEAK} = I_{OUT(MAX)} + \left(\frac{LIR}{2} \right) \times I_{OUT(MAX)}$$

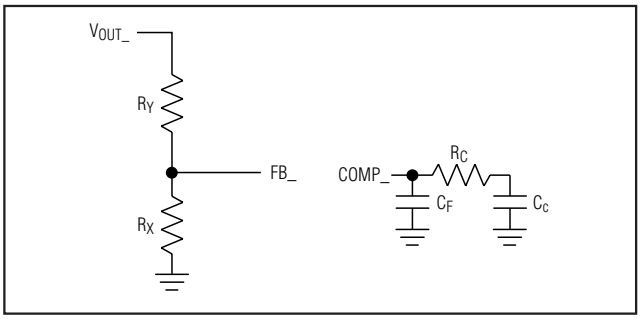


Figure 4. Feedback Divider Network and Compensation Circuitry

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{1}{V_{IN}} \sqrt{(I_{OUT1})^2 \times V_{OUT1} \times (V_{IN} - V_{OUT1}) + (I_{OUT2})^2 \times V_{OUT2} \times (V_{IN} - V_{OUT2})}$$

Output Capacitor Selection

The key selection parameters for the output capacitor are the actual capacitance value, the ESR, the ESL, and the voltage-rating requirements, which affect the overall stability, output ripple voltage, and transient response.

The output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's ESR, and the voltage drop across the capacitor's ESL caused by the current into and out of the capacitor:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output voltage ripple from the ESR is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

The output voltage ripple because of the output capacitance is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

The output voltage ripple due to the ESL of the output capacitor is:

$$V_{RIPPLE\ (ESL)} = V_{IN}\left[\frac{ESL}{ESL + L}\right]$$

I_{P-P} is the peak-to-peak inductor current:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

These equations are suitable for initial capacitor selection to meet the ripple requirement, but final values can depend on the relationship between the LC double-pole frequency and the capacitor ESR zero. Generally, the ESR zero is higher than the LC double pole. However, it is preferable to keep the ESR zero as close to the LC double pole as possible to negate the sharp phase shift of the typically high-Q double-LC pole (see the *Compensation Design* section). Solid polymer electrolytic capacitors are recommended because of their low ESR and ESL at the switching frequency. Higher output-current applications require multiple output capacitors connected in parallel to meet the output ripple voltage requirements.

The response to a load transient depends on the output capacitor. After a load transient, the output voltage instantly changes by ESR x ΔI_{LOAD} + ESL x dI/dt. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The response time depends on the closed-loop bandwidth. With a higher bandwidth, the response is faster, thus preventing the output voltage from deviating further from its nominal value. Do not exceed the capacitor's voltage or ripple-current ratings.

MOSFET Selection

The MAX1955/MAX1956 drive external, logic-level, N-channel MOSFETs as the circuit-switch elements. The key selection parameters:

On-resistance ($R_{DS(ON)}$): the lower the better.

Maximum drain-to-source voltage (V_{DSS}): should be at least 20% higher than input supply rail at the high-side MOSFET's drain.

Gate charges (Q_G, Q_{GD}, Q_{GS}): the lower the better.

Choose the MOSFETs with rated $R_{DS(ON)}$ at V_{GS} = 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET that has a conduction loss equal to switching loss at nominal input voltage and maximum output current (see below). For low-side MOSFET, make sure that it does not spuriously turn on because of dV/dt caused by high-side MOSFET turning on, as this would result in shoot-through current degrading the efficiency. MOSFETs with a lower Q_{GD}-to-Q_{GS} ratio have higher immunity to dV/dt.

For proper thermal-management design, calculate the power dissipation at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for low-side MOSFET, worst case is at VIN(MAX); for high-side MOSFET, it could be either at VIN(MIN) or VIN(MAX)). High-side MOSFET and low-side MOSFET have different loss components due to the circuit operation. Low-side MOSFET operates as a zero voltage switch; therefore, major losses are: the channel conduction loss (P_{LSCC}), the body-diode conduction loss (P_{LSDC}), and the gate-drive loss (P_{LSDR}):

$$P_{LSCC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times (I_{LOAD})^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{LSDC} = 2\, I_{LOAD} \times V_F \times t_{DT} \times f_{SW}$$

where V_F is the body-diode forward-voltage drop, t_{DT} is the dead time (~25ns), and f_{SW} is the switching frequency.

Because of the zero-voltage switch operation, low-side MOSFET gate-drive loss occurs as a result of charging and discharging the input capacitance, (C_{ISS}). This loss is distributed among the average DL gate driver's pullup and pulldown resistance, (R_{DL} (0.68Ω typ)), and the internal gate resistance (R_{GATE}) of the MOSFET (~2Ω). The drive power dissipated is given by:

$$P_{LSDR} = C_{ISS} \times (V_{GS})^2 \times f_{SW} \times \frac{R_{GATE}}{R_{GATE} + R_{DL}}$$

High-side MOSFET operates as a duty-cycle control switch and has the following major losses: the channel conduction loss (P_{HSCC}), the VI overlapping switching loss (P_{HSSW}), and the drive loss (P_{HSDR}). High-side MOSFET does not have body-diode conduction loss because the diode never conducts current:

$$P_{HSCC} = \frac{V_{OUT}}{V_{IN}} \times (I_{LOAD})^2 \times R_{DS(ON)}$$

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

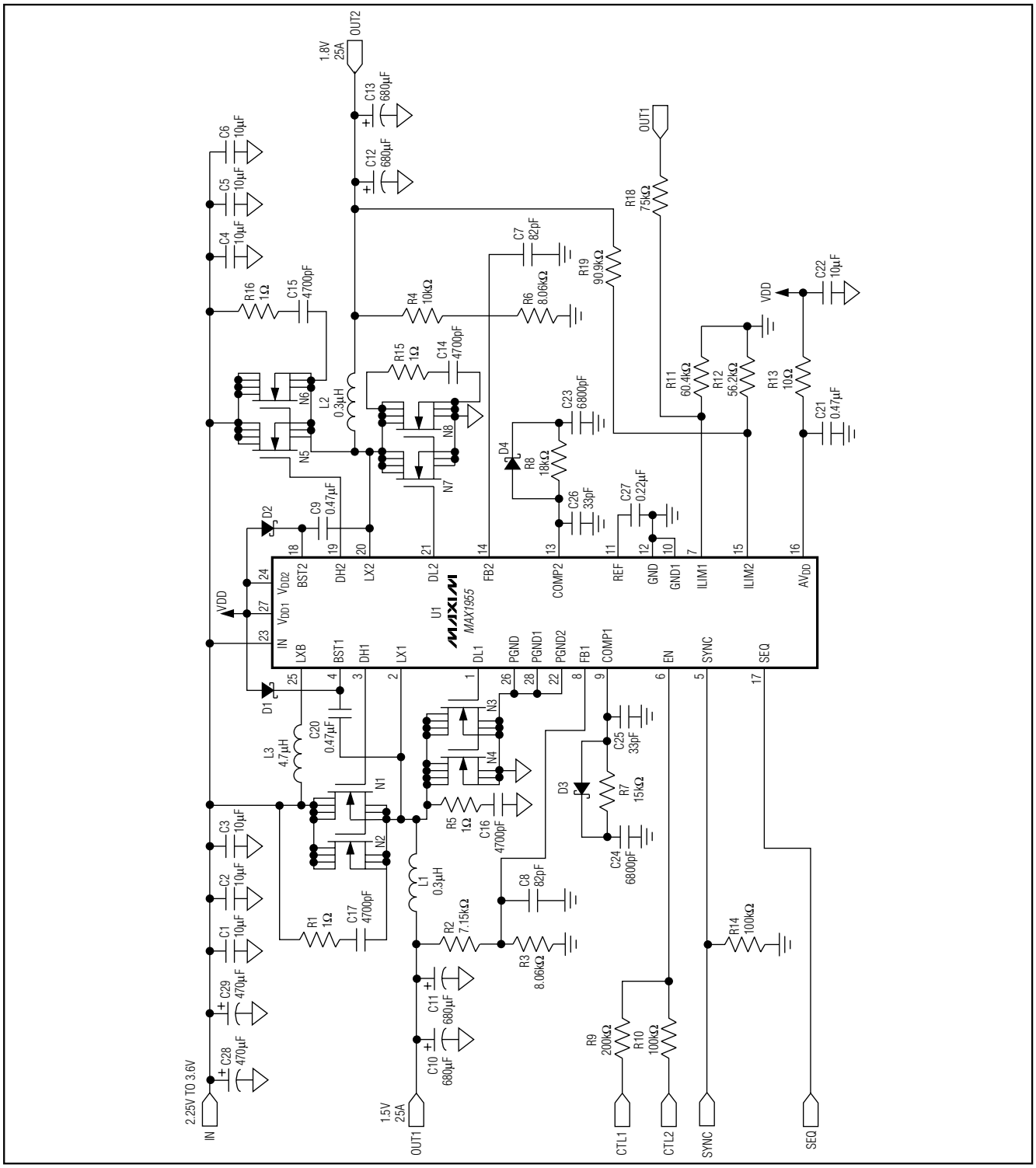


Figure 5. Typical Application Circuit

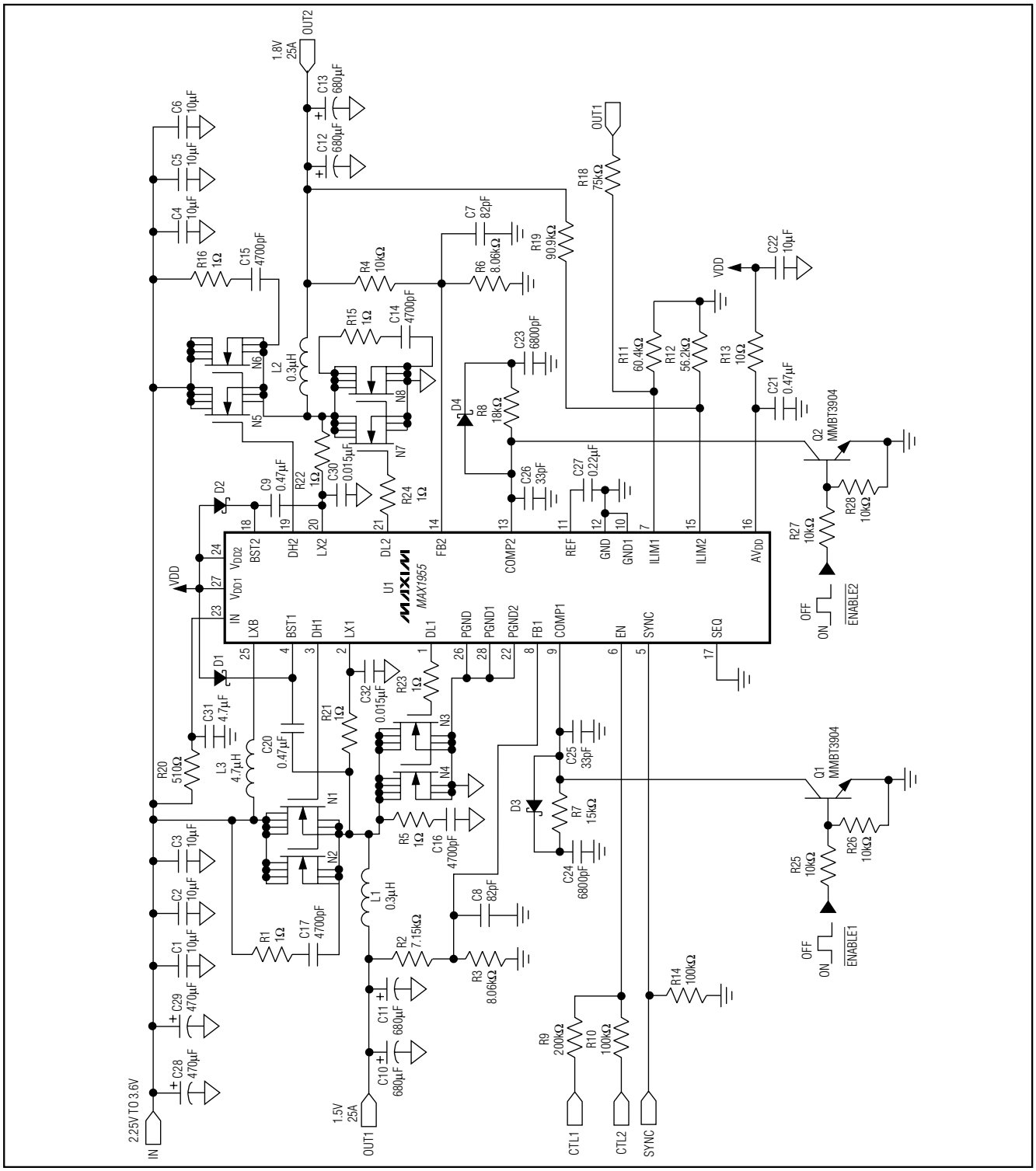


Figure 6. Independent Output On/Off Control

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

Use $R_{DS(ON)}$ at $T_{J(MAX)}$.

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times f_{SW} \times \frac{Q_{GS} + Q_{Gd}}{I_{GATE}}$$

where I_{GATE} is the average DH driver output-current determined by:

$$I_{GATE(ON)} = \frac{2.5}{R_{DH} + R_{GATE}}$$

where R_{DH} is the high-side MOSFET driver's on-resistance (1Ω typical) and R_{GATE} is the internal gate resistance of the MOSFET (~2Ω):

$$P_{HSDR} = Q_G \times V_{GS} \times f_{SW} \times \frac{R_{GATE}}{R_{GATE} + R_{DH}}$$

where $V_{GS} = V_{VDD} = 5V$.

In addition to the losses above, allow about 20% more for additional losses because of MOSFET output capacitances and low-side MOSFET body-diode reverse recovery charge dissipated in the high-side MOSFET that is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specifications to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above-calculated power dissipations.

To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source, or add resistors in series with DH and DL to slow down the switching transitions. Adding series resistors increases the power dissipation of the MOSFET, so ensure that this does not overheat the MOSFET.

MOSFET Snubber Circuit

Fast switching transitions cause ringing because of resonating circuit parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX's rising and falling transitions and can interfere with circuit performance and generate EMI. To dampen this ringing, a series R-C snubber circuit is added across each switch. Below is the procedure for selecting the value of the series R-C circuit:

1) Connect a scope probe to measure V_{LX} to GND, and observe the ringing frequency, f_R.
2) Find the capacitor value (connected from LX to GND) that reduces the ringing frequency by half.

   The circuit parasitic capacitance (C_{PAR}) at LX is then equal to 1/3 the value of the added capacitance above. The circuit parasitic inductance (L_{PAR}) is calculated by:

$$L_{PAR} = \frac{1}{(2\pi f_R)^2 \times C_{PAR}}$$

The resistor for critical dampening (R_{SNUB}) is equal to $2\pi \times f_R \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion.

The capacitor (C_{SNUB}) should be at least 2 to 4 times the value of the C_{PAR} in order to be effective. The power loss of the snubber circuit is dissipated in the resistor (P_{RSNUB}) and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times (V_{IN})^2 \times f_{SW}$$

where V_{IN} is the input voltage and f_{SW} is the switching frequency. Choose an R_{SNUB} power rating that meets the specific application's derating rule for the power dissipation calculated.

Boost-Supply Diode and Capacitor

A low-current Schottky diode, such as CMSSH-3 from Central Semiconductor, works well for most applications. Do not use large-power diodes, because higher junction capacitance can charge up the BST to LX voltage and can exceed the device rating of 6V. The boost capacitor should be 0.1µF to 4.7µF, depending on the input and output voltages, external components, and PC board layout. The boost capacitance should be as large as possible to prevent it from charging to excessive voltage, but small enough to adequately charge during the minimum low-side MOSFET conduction time, which happens at maximum operating duty cycle (this occurs at minimum input voltage). In addition, ensure that the boost capacitor does not discharge to below the minimum gate-to-source voltage required to keep the high-side MOSFET fully enhanced for lowest on-resistance. This minimum gate-to-source voltage $V_{GS(MIN)}$ is determined by:

$$V_{GS(MIN)} = V_{VDD} - \frac{Q_G}{C_{BOOST}}$$

where V_{VDD} is 5V, Q_G is the total gate charge of the high-side MOSFET, and C_{BOOST} is the boost capacitor value.

Compensation Design

The MAX1955/MAX1956 use a voltage-mode control scheme that regulates the output voltage by comparing the error amplifier output (COMP) with a fixed internal ramp to produce the required duty cycle. The inductor and output capacitor create a double pole at the resonant frequency, which has a gain drop of 40dB per decade and phase shift of 180°. The error amplifier

must compensate for this gain drop and phase shift in order to achieve a stable high-bandwidth closed-loop system.

The basic regulator loop consists of a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain set by V_{IN}/V_{RAMP}, with a double pole set by the inductor and output capacitor and a single zero set by the output capacitor (C_{OUT}) and its ESR. Equations that define the power modulator follow:

The DC gain of the power modulator:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}$$

where V_{RAMP} = 1V. The double-pole frequency because of the inductor and output capacitor is:

$$f_{PMOD} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

The zero frequency because of the output capacitor's ESR is:

$$f_{ZESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The output capacitor is usually composed of several same-value capacitors connected in parallel. With n capacitors in parallel, the output capacitance is:

$$C_{OUT} = n \times C_{EACH}$$

The total ESR is:

$$ESR = \frac{ESR_{EACH}}{n}$$

The ESR zero (f_{ZESR}) for a parallel combination of capacitors is the same as that of an individual capacitor. The feedback divider has a gain of $G_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 0.8V.

The transconductance error amplifier has DC gain $G_{EA(dc)}$ of 80dB. A dominant pole is set by the compensation capacitor (C_C), the amplifier-output resistance ($R_O \cong 5M\Omega$), and the compensation resistor (R_C):

$$f_{PEA} = \frac{1}{2\pi \times C_C \times (R_O + R_C)}$$

A zero is set by the compensation resistor and the compensation capacitor:

$$f_{ZEA} = \frac{1}{2\pi \times C_C \times R_C}$$

The total closed-loop gain must equal unity at the crossover frequency, where the crossover frequency should be higher than f_{ZESR}, so that the -1 slope is used to cross over at unity gain. Also, the crossover frequency should be less than or equal to 1/5 the switching frequency:

$$f_{ZESR} < f_C < \frac{f_{SW}}{5}$$

The loop-gain equation at the crossover frequency is:

$$\frac{V_{FB}}{V_{OUT}} \times G_{EA(fc)} \times G_{MOD(fc)} = 1$$

where:

$$G_{EA(fc)} = g_{mEA} \times R_C, \text{ and}$$

$$G_{MOD(fc)} = G_{MOD(DC)} \times (f_{PMOD})^2 / (f_{ESR} \times f_C)$$

The compensation resistor (R_C) is calculated from:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(fc)}}$$

where g_{mEA} = 2mS.

Because of the underdamped (Q > 1) nature of the output LC double pole, the error amplifier compensation zero should be approximately 0.2 f_{PMOD} to provide good phase boost. C_C is calculated from:

$$C_C = \frac{5}{2\pi \times R_C \times f_{PMOD}}$$

A small capacitor (C_F) also can be added from COMP to GND to provide high-frequency decoupling. C_F adds

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

another high-frequency pole (f_{PHF}) to the error-amplifier response. This pole should be greater than 100 times the error-amplifier zero frequency in order to have negligible impact on the phase margin. This pole also should be less than half the switching frequency for effective decoupling:

$$100f_{ZEA} < f_{PHF} < 0.5f_{SW}$$

Select a value for f_{PHF} in the range given above, and then solve for C_F using the following equation:

$$C_F = \frac{1}{2\pi \times R_C \times f_{PHF}}$$

With two converters in proximity, there is a potential for crosstalk between the converters. Crosstalk can be managed by board layout and high-frequency filtering, which can be inserted by adding a high-frequency pole in the feedback network. To do so and minimize effect on phase margin, add capacitors C7 and C8 (Figure 5) with a pole frequency of:

$$f_{PFB2} = (R4 + R6) / 2\pi \times R4 \times R6 \times C7)$$

$$f_{PFB1} = (R2 + R3) / (2\pi \times R2 \times R3 \times C8)$$

Set the poles above ~4 to 5 times the crossover frequency.

Below is a numerical example to calculate the compensation values used in the typical application circuit of Figure 5:

V_{IN} = 3V (the midpoint of the input voltage range)

V_{RAMP} = 1V

V_{OUT} = 1.8V

V_{FB} = 0.8V

$I_{OUT(MAX)}$ = 25A

C_{OUT} = 2 x 680µF

ESR = 0.008Ω / 2 = 0.004Ω

L = 0.3µH

g_{mEA} = 2mS

f_{SW} = 600kHz

$$f_{PMOD} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

$$= \frac{1}{2\pi \times \sqrt{0.3 \times 10^{-6} \times 1360 \times 10^{-6}}} = 7.879kHz$$

$$f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} = \frac{1}{2\pi \times 1360 \times 10^{-6} \times 0.004}$$

$$= 29.3kHz$$

Pick the crossover frequency (f_C) in the range $f_{ZESR} < f_C < f_{SW}/5$:

$$29.3kHz < f_C < 120kHz$$

Select f_C = 100kHz (this meets the criteria above), and the bandwidth is high enough for good transient response.

The power-modulator gain at f_C is:

$$G_{MOD(fc)} = \frac{V_{IN}}{V_{RAMP}} \times \frac{(f_{PMOD})^2}{f_{ZESR} \times f_C}$$

$$= \frac{3}{1} \times \frac{(7.879kHz)^2}{29.3kHz \times 100kHz} = 0.0477$$

Pick R_X = 8.06kΩ, then R_Y = 10kΩ (see the *Setting the Output Voltage* section).

$$R_C = \frac{V_{OUT}}{g_{mEA} \times G_{MOD(fc)} \times V_{FB}}$$

$$= \frac{1.8}{0.002 \times 0.8 \times .0636} = 17.6k\Omega$$

Select R_C = 18kΩ (nearest standard resistor value).

$$C_C = \frac{5}{2\pi \times R_C \times f_{PMOD}} = \frac{5}{2\pi \times 18k\Omega \times 7.879kHz} = 5620pF$$

Select C_C = 6800pF (rounded up to the next standard capacitor value).

Select f_{PHF} in the range $100f_{ZEA} < f_{PHF} < 0.5f_{SW}$. Hence:

$$157.6kHz < f_{PHF} < 300kHz$$

Select f_{PHF} = 250kHz, and then solve for C_F:

$$C_F = \frac{1}{2\pi \times R_C \times f_{PHF}} = \frac{1}{2\pi \times 18k\Omega \times 250kHz} = 33pF$$

A summary of feedback divider and compensation components follows:

R_X = 8.06kΩ

R_Y = 10kΩ

R_C = 18kΩ

C_C = 6800pF

C_F = 33pF

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

Applications Information

PC Board Layout Guidelines

Careful PC board layout is important in any switching regulator. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

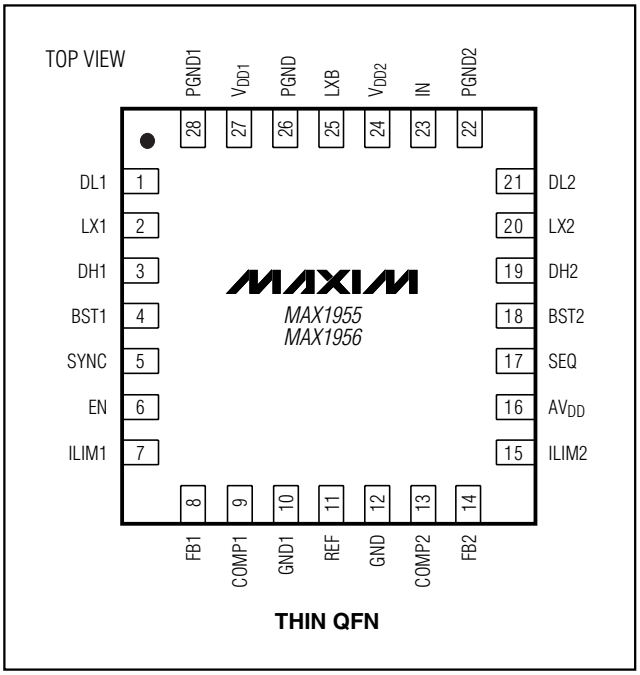
1) Place decoupling capacitors as close as possible to the IC pins.
2) Keep a separate power ground plane (connect to the sources of the low-side MOSFETs, the input and output capacitors, and PGND_ pins). Connect the input decoupling capacitors across the drain of the high-side MOSFETs and the source of the low-side MOSFETs. The signal ground plane (connected to the GND pin) is connected to the power ground plane at a single point. Keep the high-current paths as short as possible.
3) Connect the drains of the MOSFETs to a large land area to help cooling the devices to further improve efficiency and long-term reliability.
4) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
5) Route high-speed switching nodes (LX_) away from sensitive analog areas (FB_, COMP_).

For a sample PC board layout, refer to the MAX1955 evaluation kit. Table 2 lists typical application circuit components.

Table 2. Typical Application Circuit Components

DESIGNATION	QTY	DESCRIPTION
C10–C13	4	680µF, 2.5V POSCAPs Sanyo 2R5TPD680M8
C28, C29	2	470µF, 6.3V POSCAPs Sanyo 6TPB470M
D1–D4	4	Schottky diodes (SOT 323) Central CMSSH-3
L1, L2	2	0.3µH, 35A inductors Sumida CDEP125(U)-0R3
L3	1	4.7µH inductor TDK LDR655312T-4R7W
N1, N2, N5, N6	4	N-channel MOSFETs Vishay Si7892DP
N3, N4, N7, N8	4	N-channel MOSFETs Vishay Si4842DY

Pin Configuration



Chip Information

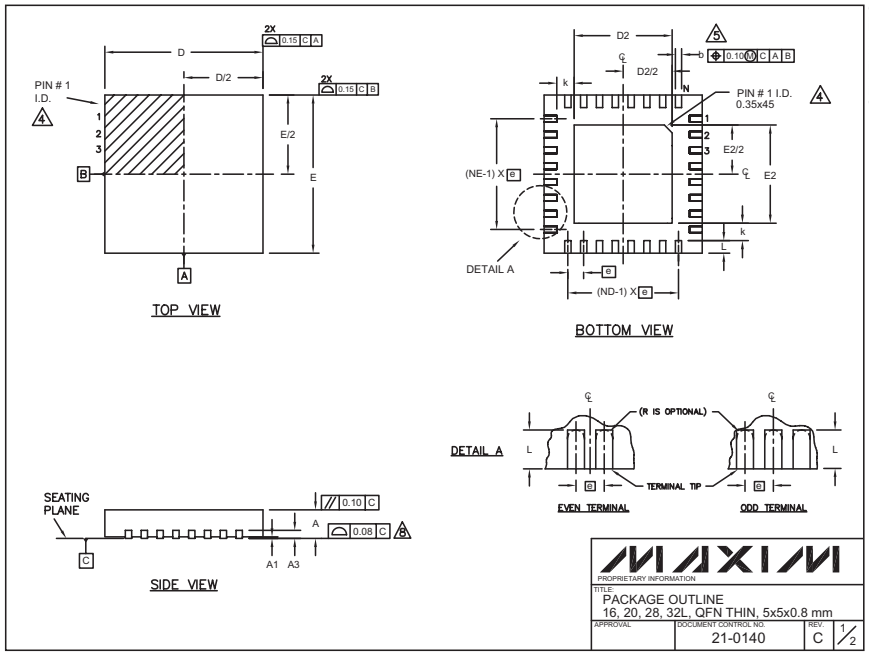
TRANSISTOR COUNT: 8694

PROCESS: BiCMOS

1.6V to 5.5V Input, 0.5% Accurate, Dual 180° Out-of-Phase Step-Down Controllers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE
PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0140
REV.
C
2/2